

Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Currently Amended) A semiconductor memory device comprising testmode circuitry, adapted to maintain a pair of bitlines coupled to a memory cell within the device to the same logic state during operation of the testmode circuitry by forwarding a direct current from a voltage source to each of the pair of bitlines through a path that comprises a respective local interconnect structure, wherein the bitlines are not maintained at the logic state during ordinary operation of the device.
2. (Canceled)
3. ~~2~~ 3. (Original) The semiconductor memory device as recited in claim ~~1~~, further comprising a user-determined voltage from the voltage source.
4. ~~3~~ 4. (Original) The semiconductor memory device as recited in claim ~~1~~, wherein the direct currents flow for a user-determined time.
5. (Canceled)
6. ~~4~~ 5. (Original) The semiconductor memory device as recited in claim ~~1~~, wherein each of the local interconnect structures comprises at least one contact through which the respective direct current passes when the bitlines are at the same logic state.
7. ~~5~~ 6. (Original) The semiconductor memory device as recited in claim 1, wherein the testmode circuitry is further adapted to force the pair of bitlines to circuit ground.
8. ~~6~~ 7. (Original) The semiconductor memory device as recited in claim 1, wherein the testmode circuitry is further adapted to hold the bitlines at the same logic state for a user-determined length of time.
9. ~~7~~ 8. (Currently Amended) A system for testing a semiconductor memory device, said system comprising testmode circuitry within the semiconductor memory device adapted to maintain a pair of bitlines coupled to a memory cell within the memory device to the same logic state, wherein the bitlines are not maintained at the logic state during ordinary operation of the device.

- ~~8~~ <sup>10</sup> (Original) The system as recited in claim 9, wherein the testmode circuitry is adapted to force the pair of bitlines to a circuit ground potential.
- ~~9~~ <sup>11</sup> (Original) The system as recited in claim 9, wherein the testmode circuitry is further adapted to maintain the pair of bitlines at the same logic state for a user-determined length of time.
12. (Canceled)
- ~~10~~ <sup>15</sup> (Original) The system as recited in claim 9, wherein the system is adapted to test a packaged memory device.
- ~~11~~ <sup>14</sup> (Currently Amended) A method for testing a semiconductor memory device, said method comprising forcing the memory device into a logic state configuration not occurring during normal operation of the device by holding each of the bitlines at a circuit ground potential.
- ~~12~~ <sup>15</sup> (Original) The method as recited in claim ~~14~~ <sup>11</sup>, wherein said forcing comprises maintaining each of a pair of bitlines within the device at the same logic state, wherein the bitlines are complementary during normal operation of the device.
16. (Canceled)
- ~~13~~ <sup>11</sup> (Original) The method as recited in claim ~~14~~ <sup>11</sup>, wherein said forcing comprises using circuitry external to the memory device.
- ~~14~~ <sup>12</sup> (Original) The method as recited in claim ~~15~~ <sup>12</sup>, wherein said forcing comprises flowing a direct current through the memory device from a voltage source to each of the pair of bitlines.
- ~~15~~ <sup>14</sup> (Original) The method as recited in claim ~~18~~ <sup>14</sup>, wherein flowing a direct current through the memory device comprises flowing a direct current through at least one local interconnect structure of a bi-stable latch.
- ~~16~~ <sup>11</sup> (Original) The method as recited in claim ~~14~~ <sup>11</sup>, wherein said forcing comprises holding the logic state configuration not occurring during normal operation of the device for a predetermined time.

- 17 ~~21~~<sup>16</sup>. (Original) The method as recited in claim ~~20~~<sup>16</sup>, wherein said predetermined time is user-variable.
- 18 ~~22~~<sup>11</sup>. (Original) The method as recited in claim ~~14~~<sup>11</sup>, said method further comprising performing a gross functional test on the memory device prior to said forcing.
- 19 ~~23~~<sup>11</sup>. (Original) The method as recited in claim ~~14~~<sup>11</sup>, said method further comprising performing a gross functional test on the memory device after said forcing.
- 20 ~~24~~. (Original) A method of stressing a semiconductor memory device comprising passing a first direct current through a first input node of a bi-stable latch within the memory device.
- 21 ~~25~~<sup>20</sup>. (Original) The method as recited in claim ~~24~~<sup>20</sup>, wherein said passing the first direct current through the first input node comprises electrically coupling a first node within the memory device to a circuit ground potential and electrically coupling a second node within the memory device to a voltage source, wherein the first input node is arranged electrically between the first and second nodes.
- 22 ~~26~~<sup>20</sup>. (Original) The method as recited in claim ~~24~~<sup>20</sup>, said method further comprising passing a second direct current through a second input node of a bi-stable latch within the memory device.
- 23 ~~27~~<sup>22</sup>. (Original) The method as recited in claim ~~26~~<sup>22</sup>, wherein said passing the second direct current through the second input node comprises electrically coupling a third node within the memory device to a circuit ground potential and electrically coupling a fourth node within the memory device to a voltage source, wherein the second input node is arranged electrically between the third and fourth nodes.
- 24 ~~28~~<sup>20</sup>. (Original) The method as recited in claim ~~24~~<sup>20</sup>, wherein the memory device comprises an SRAM.
- 25 ~~29~~<sup>20</sup>. (Original) The method as recited in claim ~~24~~<sup>20</sup>, wherein said passing the direct current through the memory device occurs after packaging the device.